

**Amendments to the Claims**

Please replace all prior versions, and listings of claims in the application with the following listing of claims.

**Listing of claims**

Claim 1 (currently amended): Apparatus for use in a computer system comprising:  
    a bus architecture;  
    a plurality of modules connected to the bus architecture, each module being assigned an address range in a memory map of the apparatus;  
    each module comprising:  
        reception means for receiving and storing availability data indicative of the availability of modules;  
        transaction request means for producing a transaction request including target address data indicating a target location in the memory map for the transaction;  
        decoding means for decoding the target address data to produce module identity data relating to a target module, the target module having an address range in the memory map which address range includes the target address data;  
        comparison means for analysing the stored availability data corresponding to the target module identified by the module identity data; and  
        transaction means, responsive to the comparison means, for terminating the transaction request if the analysed availability data indicates that the target module is unavailable,  
    wherein, for a transaction between an initiating module and a target module, decoding of the target address is carried out in the decoding means located in said initiating module.

Claim 2 (previously presented):     Apparatus as claimed in claim 1, further comprising a control means for controlling access to the bus architecture by the modules, and wherein the transaction means is further operable to forward, to the control means, a transaction request, if the analysed availability data indicates that the target module is available.

Claim 3 (original):     A computer system comprising apparatus as claimed in claim 1.

Claim 4 (original): An integrated circuit comprising apparatus as claimed in claim 1.